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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,627	07/15/2004	Nicolas Guillarme	026032-4787	4873

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EXAMINER	
KAPLAN, HAL IRA	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/501,627	GUILLARME ET AL.	
	Examiner	Art Unit	
	Hal I. Kaplan	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-9,11,13-19,21,23-25,27,28,30,31 and 33-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-9,11,13-19,21,23-25,27,28,30,31 and 33-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *20071016*.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner would like to thank the Applicant for the time and courtesies extended in the telephonic interview on August 8, 2007. The rejections of claims 1 and 3 were discussed. The Applicants argued that there was no motivation for the combination of the Mitchell reference with the other references.

Claim Objections

1. Claim 30 is objected to because of the following informalities: Claim 30, lines 2-3, "a first positive terminal and a first negative terminal for a second positive terminal" should be "a first positive terminal and a first negative terminal for a first electrical network; a second positive terminal". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 4-9, 11, 13-19, 21, 23-25, 27, 28, 30, 31, and 33-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US patent of Carpenter et al. (6,275,958) in view of the US patent of Hemena et al. (6,160,386), and further in view of the US patent of Willis (5,598,041).

As to claims 1, 7-9, 13, 17-19, 21, 30, 31, 33, 34, and 37, Carpenter, drawn to fault detection in a redundant power converter, discloses, in Figures 5 and 6, a DC/DC voltage converter comprising: a first positive terminal (+Vin) and a first negative terminal (ground) for connection respectively to two terminals of a high-voltage electrical network; a second positive terminal (+Vout) and a second negative terminal (ground) for connection respectively to two terminals of a low-voltage electrical network (see column 1, lines 25-28); and n cells (20) connected in parallel, where n is an integer greater than unity, disposed between the first positive (+Vin) and negative (ground) terminals and between the second positive (+Vout) and negative (ground) terminals, each cell (20) comprising a chopper DC/DC converter (see column 2, lines 8-10 and 64-67, and

Figure 6), each having a first circuit branch (ground) interconnecting the first and second negative terminals, a second circuit branch including an inductor (19) and interconnecting the first (+Vin) and second (+Vout) positive terminals, chopper means comprising at least one chopper switch (S1), and a management unit (18) adapted to control OFF and ON switching of the chopper switch (S1) with a determined duty ratio (see column 1, lines 37, 46-51, and 60-63, and Figure 6). Carpenter does not disclose only one protection transistor per cell, the intrinsic diode of the transistor connected to the inductor by its cathode and to the second positive terminal by its anode, or a protection switch which is common to all of the cells.

Hemena, drawn to a parallel power system which includes over voltage protection, discloses, in Figure 3B, a non-isolated chopper DC/DC converter cell comprising a single protection transistor (102) (see column 2, lines 54-55 and column 3, lines 10-13 and 38-44). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to build the DC/DC converter of Carpenter using cells comprising a single protection transistor as taught by Hemena, in order to reduce the number of parts and the cost. Hemena does not disclose the intrinsic diode of the transistor connected to the inductor by its cathode and to the second positive terminal by its anode, or a protection switch which is common to all of the cells.

Willis discloses a MOS transistor (16) for protection of redundant DC power supplies, comprising an intrinsic diode (14) having an anode and a cathode, the anode connected to the output terminal of the circuit (see column 2, lines 23-42; column 3, lines 23-28; and Figures 1 and 2). It would have been obvious to one of ordinary skill in

the art, at the time of the invention, to use a MOS transistor connected in series between the inductor and second positive terminal of each cell of the DC/DC converter of Carpenter, and including an intrinsic diode connected to the inductor by its cathode and to the second positive terminal by its anode, in order to provide protection if there is a short circuit in the load.

As to claims 4, 6, 11, 14, and 23, in the converter of Hemena, the single protection transistor (102) in each cell (100(a)) is connected in a high-voltage portion of the cell (see Figure 3B).

As to claim 5, the protection transistor of Hemena is a MOS transistor (Q2) connected in series in the second circuit branch so as to be immediately adjacent to the first positive terminal (Vin) (see Figure 3B). The converter of Carpenter teaches a MOS protection transistor (48) connected in series in the second circuit branch so as to be immediately adjacent to the first positive terminal (+Vin), with an intrinsic diode connected to the first positive terminal by its cathode (see column 4, lines 48-51 and Figure 5). It would have been obvious to one of ordinary skill in the art, at the time of the invention, to build the converter of Carpenter in view of Hemena, as set forth above, with the MOS protection transistor of Carpenter in place of the MOS protection transistor (102) of Hemena, in order to block an overvoltage resulting from a short of the MOS protection transistor.

As to claims 15, 24, and 30, none of the prior art of record specifically discloses the 0.5% value; however, selection of values of operational levels for an electronic device are engineering decisions based upon the device's intended use and the

expected requirements of the systems with which it will interface. See MPEP §2144.04(IV)(A).

In *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), *cert. denied*, 469 U.S. 830, 225 USPQ 232 (1984), the Federal Circuit held that, where the only difference between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device.

As to claims 16, 28, and 36, none of the prior art of record specifically discloses the first and second electrical networks being components of a vehicle, but it has been held that a claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987). See MPEP §2114.

As to claim 25, Carpenter discloses more than 2 cells (see Figure 6).

As to claims 27 and 35, none of the prior art of record specifically discloses each of the cells comprising both a buck converter and a boost converter; however, Hemena discloses DC-DC converter cells without limitation as to whether they are buck, boost, or buck-boost converters (see column 1, lines 13-16), so buck-boost converters could be used.

As to claim 37, the protection switch of Willis is common to all of the DC power supplies (35), and in the cited combination of references, a single additional protection switch can be connected at the common output of all of the parallel DC/DC converter modules, each of which contains its own such protection switch.

Response to Arguments

6. Applicant's arguments, see Remarks, filed August 15, 2007, with respect to the objection to claim 6 have been fully considered and are persuasive. The objection to claim 6 has been withdrawn.

7. Applicant's arguments, see Remarks, filed August 15, 2007, with respect to the rejection(s) of claim(s) 1, 4-11, 13-21, 23-25, 27, 28, and 30-36 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the US patent of Willis (5,598,041).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal I. Kaplan whose telephone number is 571-272-8587. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on 571-272-2084. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

hik

10/28/08

MICHAEL SHERRY
SUPERVISORY PATENT EXAMINER